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			Application Number	10/718,662	
			Filing Date	November 24, 2003	
			First Named Inventor	Edwin C. Kan	
			Art Unit	2818	
			Examiner Name		
Sheet	2	of	3	Attorney Docket Number	CRF D-2768D/Kan

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
/DL/	10	"Single-Electron Devices and Their Applications," K.K. Likharev; Proceedings of the IEEE, Vol. 87, No. 4, April 1999	
	11	"Non-Volatile Si Quantum Memory with Self-Aligned Doubly-Stacked Dots," R. Ohba, N. Sugiyama, K. Uchida, J. Koga, A. Toriumi; IEEE 2000	
	12	"Modification of Indium Tin Oxide for Improved Hole Injection in Organic Light Emitting Diodes," Y. Shen, D.B. Jacobs, G.G. Malliaras, G. Koley, M.G. Spencer, A. Ioannidis; Adv. Mater. 2001, No. 16, 8/16	
	13	"Room Temperature Operation of a Quantum-Dot Flash Memory," J.J. Welser, S. Tiwari, S. Rishton, K.Y. Lee, Y. Lee; IEEE Electron Device Letters, Vol. 18, No. 6, June 1997	
	14	"Silicon Nano-Crystals Based MOS Memory and Effects of Traps on Charge Storage Characteristics," Y. Shi, S.L. Bu, X.L. Yuan, Y.D. Zheng; K. Saito, H. Ishikuro, T. Hiramoto; IEEE 1998	
	15	"A High Capacitive-Coupling Ratio (HiCR) Cell for 3 V-Only 64 Mbit and Future Flash Memories," Y.S. Hisamune, K. Kanamori, T. Kubota, Y. Suzuki, M. Tsukiji, E. Hasegawa, A. Ishitani, T. Okazawa, IEEE 1993	
	16	"Volatile and Non-Volatile Memories in Silicon with Nano-Crystal Storage," S. Tiwari, F. Rana, K. Chan, H. Hanafi, W. Chan, D. Buchanan; 1995 IEEE	
/DL/	17	"Multilevel Flash cells and their Trade-offs," B. Eitan, R. Kazerounian, A. Roy; G. Crisenza, P. Cappelletti, A. Modelli; 1996 IEEE	
/DL/ No date	18	"Modeling and Design Study of Nanocrystal Memory Devices," M. She, Y-C King, T-J King, C. Hu; Dept. of Elect. Eng. and Comp. Sciences, U. of C., Berkely, CA	
/DL/	19	"A Four-State EEPROM Using Floating-Gate Memory Cells," C. Bleiker, H. Melchior; IEEE Journal of Solid-State Circuits, Vol. SC-22, No. 3, June 1987	

Examiner Signature	/David Lam/	Date Considered	03/28/2007
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\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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